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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,103	06/30/2003	Ho Jin Cho	40296-0025	1058

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EXAMINER	
KENNEDY, JENNIFER M	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,103	CHO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) *1-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicants' amendment to the specification the objections are withdrawn.

In view of Applicants' amendment to the claims the objections are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, and 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,580,111) and Park et al. (U.S. Patent Appl. 2002/0020869) in view of Halliyal et al. (U.S. Patent No. 6,645,882).

In re claim 1, Kim et al. disclose the method for forming a capacitor of a semiconductor device, comprising the steps of:

(a) forming an oxide film (140, 142) on an interlayer insulating film (100) having a storage electrode contact plug (110);

(b) selectively etching the oxide film to form an opening exposing the top surface of the storage electrode contact plug (see Figure 5, and column 5, lines 56-62);

(c) forming a conductive layer (160) on the bottom and the inner walls of the opening;

(d) removing the oxide film to form a storage electrode (see column 6, lines 15-20);

(e) forming a dielectric film (180) on the surface of the storage electrode;

(f) annealing the dielectric film (see column 6, lines 39-45); and

(g) forming a plate electrode (190) on the dielectric film.

Kim et al. disclose the method of forming the lower electrode of titanium nitride, but do not disclose the method of forming the lower electrode of polysilicon. Park et al. disclose the method of forming the lower electrode of either polysilicon or titanium nitride (see [0020]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the lower electrode of polysilicon rather than titanium nitride, because as Park et al. teaches that polysilicon and titanium nitride are interchangeable for use as lower electrodes and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Kim et al. and Park et al. do not disclose the method wherein the dielectric film has a stacked structure of Al-rich HfO_2-Al_2O_3 film and Hf-rich HfO_2-Al_2O_3 film on the

surface of the storage electrode. Halliyal et al. disclose the method wherein the dielectric film has a stacked structure of Al-rich HfO_2-Al_2O_3 film and Hf-rich HfO_2-Al_2O_3 film on the surface of the storage electrode and annealing the dielectric film (see Figure 8, see entire disclosure, and especially column 10, line 58 through column 11 line 35, and column 12, lines 17-40, column 13, lines 30-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer of the combined Kim et al. and Park et al. by the method of Halliyal et al. because as Halliyal et al. teach the method allows for a relatively high-K dielectric to be formed without the formation of the formation of the lower k dielectric silicon oxide (see Halliyal et al. column 2, lines 45-60).

The examiner notes that Halliyal et al. in column 10, line 58 through column 11 line 35 disclose the method wherein a five layer dielectric is formed, wherein the first, third and fifth layers are formed of hafnium oxide, and the second and fourth layers are formed of aluminum oxide. Thus, the first and second layers of hafnium oxide/aluminum oxide are considered the Al-rich layer (defined by Applicants as a 1:1 ratio) and the third, fourth, and fifth layers of hafnium oxide/ aluminum oxide/hafnium oxide are considered the Hf-rich layer (defined by applicants as a ratio of hafnium oxide to aluminum oxide as a 2:1 ratio).

In re claim 4, the combined Kim et al., Park et al. and Halliyal et al. disclose the method wherein the step (e) is preformed in an ALD process and the thickness of the Al-rich HfO_2-Al_2O_3 film and the Hf-rich HfO_2-Al_2O_3 film is 5 to 30Å (hafnium oxide layer

of 10 Å and aluminum oxide layer of 10 Å) and 10 to 100Å, respectively (two hafnium oxide layers of10 Å and one aluminum oxide layer of 10 Å; see Halliyal et al. column 10, line 58 through column 11 line 35).

In re claim 8, the combined Kim et al., Park et al. and Halliyal et al. disclose the method wherein a ratio of HfO_2 : Al2O3 in the Al-rich HfO_2-Al_2O_3 film ranges from (1 cycle: 1 cycle) ~ (9 cycle: 1 cycle). As explained above, Halliyal et al. disclose the first and second layers of hafnium oxide/aluminum oxide are considered the Al-rich layer formed by a 1:1 ratio.

In re claim 9, the combined Kim et al., Park et al. and Halliyal et al. disclose the method wherein a ratio of HfO_2: Al_2O_3 in the Hf-rich HfO_2-Al_2O_3 film ranges from (9 cycle: 1 cycle) ~ (2 cycle: 1 cycle). As explained above, Halliyal et al. disclose the third, fourth, and fifth layers of hafnium oxide/ aluminum oxide/hafnium oxide are considered the Hf-rich layer formed by a ratio of hafnium oxide to aluminum oxide ain a 2:1 ratio.

In re claim 10, the combined Kim et al., Park et al. and Halliyal et al. disclose the method wherein the step (f) is performed at a temperature ranges from 500 to 900°C under oxygen or nitrogen gas atmosphere for 1 to 10 minutes (see Halliyal et al. column 13, lines 30-50 and column 14, lines 40-50).

In re claim 11, the combined Kim et al., Park et al. and Halliyal et al. disclose and the method wherein the step (f) is performed in a furnace at a 500 to 900°C under oxygen, nitrogen or N_2O gas atmosphere, but do not explicitly disclose the time for heating. The examiner notes that Applicant does not teach that the annealing time solves any stated problem or is for any particular purpose. Therefore, the annealing

time range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the dielectric for 10 to 60 minutes, since the invention would perform equally well when the annealing occurs for a few minutes or 10 minutes and since Halliyal et al. teaches the time for annealing can be selectively controlled (see column 14, lines 40-50), and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 12, the combined Kim et al., Park et al. and Halliyal et al. disclose the method wherein the step (g) is a CVD process for forming the plate electrode using a material selected from the group consisting of TaN, TiN, WN, W, Pt, Ru, Ir, doped polysilicon, and combinations thereof (see Kim et al. column 6, lines 45-50).

In re claim 13, Kim et al. disclose the method for forming a capacitor of a semiconductor device, comprising the steps of:

(a) forming an oxide film (140, 142) on an interlayer insulating film (100) having a storage electrode contact plug (110);

(b) selectively etching the oxide film to form an opening exposing the top surface of the storage electrode contact plug (see Figure 5, and column 5, lines 56-62);

(c) forming a conductive layer (160) on the bottom and the inner walls of the opening;

(d) removing the oxide film to form a storage electrode (see column

6, lines 15-20);

(e) forming a dielectric film (180) on the surface of the storage electrode;

(f) annealing the dielectric film (see column 6, lines 39-45); and

(g) forming a plate electrode (190) on the dielectric film.

Kim et al. disclose the method of forming the lower electrode of titanium nitride, but do not disclose the method of forming the lower electrode of polysilicon. Park et al. disclose the method of forming the lower electrode of either polysilicon or titanium nitride (see [0020]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the lower electrode of polysilicon rather than titanium nitride, because as Park et al. teaches that polysilicon and titanium nitride are interchangeable for use as lower electrodes and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Kim et al. and Park et al. do not disclose the method wherein the dielectric film is a Al-rich HfO_2-Al_2O_3 film on the surface of the storage electrode. Halliyal et al. disclose

the method wherein the dielectric film is a Al-rich HfO_2-Al_2O_3 film (see Figure 8, see entire disclosure, and especially column 10, line 58 through column 11 line 35, and column 12, lines 17-40, column 13, lines 30-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer of the combined Kim et al. and Park et al. by the method of Halliyal et al. because as Halliyal et al. teach the method allows for a relatively high-K dielectric to be formed without the formation of the formation of the lower k dielectric silicon oxide (see Halliyal et al. column 2, lines 45-60).

The examiner notes that Halliyal et al. in column 10, line 58 through column 11 line 35 disclose the method wherein a five layer dielectric is formed, wherein the first, third and fifth layers are formed of hafnium oxide, and the second and fourth layers are formed of aluminum oxide. Thus, the first and second layers of hafnium oxide/aluminum oxide are considered the Al-rich layer (defined by Applicants as a 1:1 ratio).

In re claim 14, Kim et al. disclose the method for forming a capacitor of a semiconductor device, comprising the steps of:

(a) forming an oxide film (140, 142) on an interlayer insulating film (100) having a storage electrode contact plug (110);

(b) selectively etching the oxide film to form an opening exposing the top surface of the storage electrode contact plug (see Figure 5, and column 5, lines 56-62);

(c) forming a conductive layer (160) on the bottom and the inner walls of the opening;

(d) removing the oxide film to form a storage electrode (see column column 6, lines 15-20);

(e) forming a dielectric film (180) on the surface of the storage electrode;

(f) annealing the dielectric film (see column 6, lines 39-45); and

(g) forming a plate electrode (190) on the dielectric film.

Kim et al. disclose the method of forming the lower electrode of titanium nitride, but do not disclose the method of forming the lower electrode of polysilicon. Park et al. disclose the method of forming the lower electrode of either polysilicon or titanium nitride (see [0020]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the lower electrode of polysilicon rather than titanium nitride, because as Park et al. teaches that polysilicon and titanium nitride are interchangeable for use as lower electrodes and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Kim et al. and Park et al. do not disclose the method wherein the dielectric film has a stacked structure of a Al_2O_3 film and Hf-rich HfO_2-Al_2O_3 film on the surface of the storage electrode. Halliyal et al. disclose the method wherein the dielectric film has a stacked structure of a Al_2O_3 film and Hf-rich HfO_2-Al_2O_3 film on the surface of the

storage electrode and annealing the dielectric film (see Figure 8, see entire disclosure, and especially column 10, line 58 through column 11 line 35, and column 12, lines 17-40, column 13, lines 30-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer of the combined Kim et al. and Park et al. by the method of Halliyal et al. because as Halliyal et al. teach the method allows for a relatively high-K dielectric to be formed without the formation of the formation of the lower k dielectric silicon oxide (see Halliyal et al. column 2, lines 45-60).

The examiner notes that Halliyal et al. in column 10, line 58 through column 11 line 35 disclose the method wherein a five layer dielectric is formed, wherein the first, third and fifth layers are formed of hafnium oxide, and the second and fourth layers are formed of aluminum oxide. Thus the first layer of aluminum oxide is considered the Al_2O_3 film, and the third, fourth, and fifth layers of hafnium oxide/ aluminum oxide/hafnium oxide are considered the Hf-rich layer (defined by applicants as a ratio of hafnium oxide to aluminum oxide as a 2:1 ratio).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,580,111; referred to as Kim '111), Park et al. (U.S. Patent Appl. 2002/0020869), and Halliyal et al. (U.S. Patent No. 6,645,882) in view of Kim et al. (U.S. Patent No. 6,165,841; referred to as Kim '841).

Kim '111, Park et al., and Halliyal et al. disclose the method as claimed and rejected above, but do not disclose the method further comprising the step of cleaning

the surface of the storage electrode with a cleaning solution of NH_4OH : H_2O_2 : H_2= 1 : (4 ~ 5) : (20 ~ 50) after the step (d) to form an oxide film. Kim '841 disclose the method comprising the step of cleaning the surface of the storage electrode with a cleaning solution of NH_4OH : H_2O_2 : H_2= 1 : (4 ~ 5) : (20 ~ 50) prior to forming a dielectric in order to form an oxide film (see column 6, lines 12-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the cleaning method of Kim '841 in the combined method of Kim '111, Park et al. and Halliyal et al. in order to remove particulate metal impurities and organic contaminants on the wafer.

Neither, Kim '111, Park et al., Halliyal et al., nor Kim '841 disclose the thickness of the oxide formed. The examiner notes that Applicant does not teach that the oxide thickness solve any stated problem or are for any particular purpose. Therefore, the oxide thickness lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide of 3 to 5 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,580,111), Park et al. (U.S. Patent Appl. 2002/0020869), and Halliyal

et al. (U.S. Patent No. 6,645,882) in view of Kher et al. (U.S. Patent Appl. 2003/0232501).

Kim et al., Park et al., and Halliyal et al. disclose the method as claimed and rejected above, but do not disclose the method further comprising the step of cleaning the surface of the storage electrode with an HF or BOE solution and performing an RTO process after the step(d) to form an oxide film having a thickness ranging from 8 to 15Å. Kher et al. disclose the method comprising the step of cleaning the surface of the storage electrode with an HF or BOE solution and performing an RTO process prior to forming the capacitor dielectric to form an oxide film (see paragraph [0035],[0069-0071] and [0020]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clean the surface of the silicon with an HF or BOE solution and performing an RTO process prior to forming the dielectric, because as Kher et al. teaches this method allows for a lower surface roughness (see [0006]) which allows for conformal layers in high aspect ratio features in high density devices.

Neither, Kim et al., Park et al., Halliyal et al., nor Kher et al. disclose the thickness of the oxide formed. The examiner notes that Applicant does not teach that the oxide thickness solve any stated problem or are for any particular purpose. Therefore, the oxide thickness lacks criticality in the claimed invention and does not produce unexpected or novel results. Kher et al. teaches that the rapid thermal oxidation can occur for anywhere from 5 to 10 seconds and at a temperature of 850 to 900 °C. Since the oxide thickness is a function of temperature and time of oxidation,

Kher et al. teach one could selectively choose the conditions to form the optimal oxide thickness. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide of 8 to 15 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,580,111), Park et al. (U.S. Patent Appl. 2002/0020869), and Halliyal et al. (U.S. Patent No. 6,645,882) in view of Londergan et al. (U.S. Patent No. 6,720,259).

Kim et al., Park et al., and Halliyal et al. disclose the method as claimed and rejected above, but do not disclose the method wherein the ALD process or the CVD process performed at a temperature of 150 to 600°C and step (e) is performed in an ALD process using $Al(CH_4)_3$ as an Al source, $HfCl_4$ as an Hf source and H_2O, O_3, O_2 and N_2O as an O source one cycle for Al_2O_3 ALD process comprising Al pulse, N_2 purge, O pulse and N_2 purge, and one cycle of HfO_2 of the ALD process comprising Hf pulse, N2 purge, O pulse and N_2 purge processes. Londergan et al. disclose the method wherein the ALD process or the CVD process performed at a temperature of 150 to 600°C (see column 8, lines 5- 15) and utilizing an ALD process using $Al(CH_4)_3$ as an Al source, $HfCl_4$ as an Hf source and H_2O, O_3, O_2 and N_2O as an O source one cycle for Al_2O_3 ALD process comprising Al pulse, N_2 purge, O pulse and N_2 purge, and

one cycle of HfO_2 of the ALD process comprising Hf pulse, N2 purge, O pulse and N_2 purge processes (see 1, lines 30-45, column 2, lines 5-17, column 3, line 53 through column 4, line 13, and column 5, line 40-46, column 8, lines 5 through 42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the precursors of Londergan et al. because they are conditions and know precursors that allow for the formation of a high-k dielectric and an increase in capacitance.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,580,111), Park et al. (U.S. Patent Appl. 2002/0020869) and Halliyal et al. (U.S. Patent No. 6,645,882) in view of Conley Jr. et al. (U.S. Patent No. 6,686,212).

Kim et al., Park et al. and Halliyal et al disclose the method as claimed and rejected above, but do not disclose the method wherein the step (e) is an ALD process using a Hf source selected from the group consisting of $HfCl_4$, $Hf[N(C_2H_5)_2]_4$, $Hf[N(CH_3)_2]_4$, $Hf[N(CH_3)(C_2H_5)]_4$, $Hf[OC(CH_3)_3]_4$, $Hf(NO_3)_3$, and combinations thereof, and an O source selected from the group consisting of H_2O, O_2, N_2O, O_3, and combinations thereof, one cycle of HfO_2 of the ALD process comprising Hf pulse, N_2 purge, O pulse and N_2 purge in. Conley Jr. et al. disclose the method of forming an hafnium oxide layer by an ALD process using a Hf source selected from the group consisting of $HfCl_4$, $Hf[N(C_2H_5)_2]_4$, $Hf[N(CH_3)_2]_4$, $Hf[N(CH_3)(C_2H_5)]_4$, $Hf[OC(CH_3)_3]_4$, $Hf(NO_3)_3$, and combinations thereof, and an O source selected from the group

consisting of H_2O, O_2, N_2O, O_3, and combinations thereof, one cycle of HfO_2 of the ALD process comprising Hf pulse, N_2 purge, O pulse and N_2 purge in (see column 3, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the precursors of Conley Jr. et al. because they allow for the formation of a smooth high-k dielectric.

Response to Arguments

Applicants' arguments filed February 15, 2005 have been fully considered but they are not persuasive.

Applicants' arguments with respect to the amended independent claims 1,13, and 14, which require polysilicon, have been considered but are moot in view of the new ground(s) of rejection.

Applicants' argument with respect to the combination of Kim '11 and Halliyal is not persuasive. Applicants argue that Halliyal discloses a dielectric film used for a gate electrode, not a storage electrode. The examiner relies on Kim to disclose the storage electrode, and relies on Halliyal to disclose a dielectric material as claimed. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner notes that while Halliyal discloses utilizing the dielectric for a gate electrode, one of ordinary skill in the art would know that the dielectric of Halliyal, which has a high dielectric constant, could be also used for other capacitors such as DRAMs that require high dielectric constant materials. The examiner notes that the motivation,"It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer of Kim et al. by the method of Halliyal et al. because as Halliyal et al. teach the method allows for a relatively high-K dielectric to be formed without the formation of the formation of the lower k dielectric silicon oxide (see Halliyal et al. column 2, lines 45-60)", was clearly set forth in the non-final office action. The problems of forming a low dielectric oxide layer, as discussed in Halliyal et al., are also applicable to other devices, such as DRAM capacitors, requiring high dielectric constant materials to ensure high capacitance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al. (Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition, 128-130) disclose that a silicon oxide is formed on the surface of the substrate during SC-1 cleaning.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk